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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,149	02/27/2002	Joseph Winkles	95-520	6606

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EXAMINER	
WONG, WARNER	
ART UNIT	PAPER NUMBER
2616	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/083,149	WINKLES ET AL.	
	Examiner	Art Unit	
	WARNER WONG	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 2 is objected to because of the following informalities: on line 6, the limitation "one of the output buffer" is may lead to misinterpretation that there are more than one output buffer, with its antecedent described in claim 1, line 7, "an output buffer". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 rejected under 35 U.S.C. 103(a) as being unpatentable over McConnell (US 6,988,161).

Regarding claims 1 and 6, McConnell describes a method/channel adapter (fig. 2, Infiniband network with channel adapters matching applicant's fig. 1), the method comprising:

receiving a link management packet from a link partner and in response selecting, according to InfiniBand protocol, a selected active link width of a physical link [and memory for storing port configuration settings] (col. 10, lines 16-64, using unique Management Datagram (MAD) along with Subnet Management Packets (SMP) to select and set port configuration to memory such as the Active Link Width. In col. 10, lines 19-23, it explicitly recites physical links, which are different from link widths);

[link layer module with bus controller for] setting a circuit, configured for selectively switching frame data of a prescribed maximum link width to a selected one of a plurality of available link widths, to the selected active link width (fig. 5-6 & col. 10, lines 16-64, selecting port's Active Link Width to either 1x, 4x or 12x, where the end node's port performs multiplexing means for combining packets of VL 0-15 as shown in fig. 6);

receiving the frame data from an output buffer according to the prescribed maximum link width (fig. 6 & col. 9, line 56 to col. 10, line 5, receiving data packets 310 (frame data) from receive VL's FIFO (output) buffers according to the set (maximum) Active Link Width);

outputting the frame data from the circuit to a transmit bus according to the selected active link width (col. 9, line 56-62, transmitting data packets 310 from the multiplexing means of fig. 6 according to the set Active Link Width);

McConnell describes the above-mentioned circuit as a selector, and depicts the circuit at the port in fig. 6 to have many I/O queues going to/from a transmitter or receiver for transmission over a physical link to a remote transmitter/receiver, but fails to explicitly describe the circuit as a multiplexer circuit.

However, it would have been obvious to one with ordinary skill in the art at the time of invention by applicant to understand that the circuit portrayed by McConnell is a multiplexer circuit. The definition of a multiplexing circuit is a circuit for selecting from many I/O going to/from a serial I/O, especially for transmission.

3. Claims 2-5, 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over McConnell as applied to claims 1 and 6 above respectively, and further in view of Bunton (US 6,961,347).

Regarding claims 2 and 7, McConnell describes that the multiplexer circuit includes a first multiplexer for outputting the frame data onto a first output according to a first of the available link widths, and the multiplexer circuit configured for switching the frame data onto a second output according to a second of the available link widths, the setting step including selecting one of the output buffer, the first output, and the second output for transfer of the frame data according to the selected active link Width (fig. 6, multiplexing means (circuit) which can (first) multiplexes a number of VLs holding packet data 310 (frame data) as a first output when set to a (first) link width, and can (second) multiplexes a different number of VLs holding packet data 310 (frame data) as a second output when set to another (second) selected link width, where setting up the Active Link Width to 1x, 4x or 12x determines the number of supported subsets (or all) of VLs carrying data).

McConnell suggests one multiplexing functionality which can multiplexes the VLs differently according to link width as described above, but fails to describe a separate/second multiplexer circuit, distinct from the first multiplexer, for switching the frame data onto a second output according to a second of the available link widths.

Bunton describes an Infiniband interconnection transmitter which has two or more distinct multiplexer circuits (fig. 10 & 11) for switching the frame data into the first/second output according to a first/second of the available link widths (fig. 9 & col.

10, lines 17-23, each multiplexer's output is assigned its own available, equal portion of 1 lane of the mixed link width interconnection).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to use a second multiplexer as in Bunton for switching data onto a second output according it its available link width for the Infiniband channel adapter of McConnell.

The motivation for combining the teachings is that it can decrease the design and manufacturing costs for high bandwidth data links in implementing Infiniband physical layer (Bunton, col. 3, lines 40-41 & col. 4, lines 12-14).

Regarding claims 3 and 8, McConnell describes a prescribed number of registers, corresponding to the prescribed maximum link width, for storing respective units of the frame data, the outputting step including outputting the frame data units in a sequence relative to the selected active link width (fig. 6 & col. 10, lines 2-5, VL FIFOs (registers) for storing data packets 310 (frame data) to be sent in 1x, 4x or 12 link width, inherently mapped in sequence to be multiplexed and transmitted).

Regarding claims 4 and 9, McConnell describes that the second multiplexer circuit is configured for grouping the frame data units into a plurality of unit groups, the outputting step including causing the second multiplexer circuit to output each of the unit groups in sequence based on the sequencing signals (fig. 6 & col. 10, lines 6-10, where the (second) multiplexing means (circuit) multiplexes (groups) data packets 310 (frame data), the step of multiplexing the subset of VLs for transmission of a link is inherently in order (sequence) based on selected VLs (sequencing signals)).

Regarding claims 5 and 10, McConnell describes that the outputting step includes outputting from the first multiplexer a corresponding one of the frame data units in sequence (fig. 6 & col. 10, lines 6-10, where the (first) multiplexing means (multiplexer) outputs data packets 310 (frame data) from the VL FIFOs in order (sequence)).

Response to Arguments

4. Applicant's arguments filed 1/24/07 regarding claims 1 and 6 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 2-5 and 7-10 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 1, on p. 5 last paragraph, the applicants argues that "Even if McConnell et al. can be consider to have a multiplexing circuit, there is no disclosure or suggestion of a multiplexer circuit receiving the frame data from an output buffer according to the prescribed maximum link with, and setting the multiplexer circuit to the selected link width." The examiner respectfully disagrees.

As responded in the previous Office Action, McConnell suggested a multiplexing functionality (fig. 6) for receiving frame data from a plurality of send Queues 510A-510N (output buffer) according to the LinkWidthSupported field value set for 4x (max. link width, as opposed to 1:1x only, 2:4x only, 2:1, see col. 10, lines 32-36). The LinkWidthSupported value reports the number of lanes supported by the transmitting

port 610 (see col. 10, lines 34-35), hence setting how the multiplexing process switches input data from send queues 510.

On p. 6 paragraph 1, the applicants argue the McConnell fails to suggest "transfer of the data according to the appropriate widths and the appropriate sequence". The issue of "transfer of the data according to the appropriate widths" has just been addressed above. The examiner noted that the transfer of data according to the appropriate sequence is not in the claimed 1's language.

On p. 6 paragraph 1, the applicants further argue that "there is no concept of maximum lane width in the virtual lane". The examiner notes that the claim language differs from this statement, where the limitations "selectively switching frame data of a prescribed maximum link width to a selected one of a plurality of available link widths, to the selected active link width" can be interpreted as per the response to argument or Office Action above (see also col. 9, lines 66-67 & col. 10, lines 33, where # of lanes = width per description from the cited columns/lines).

On p. 6 paragraph 4, the applicant is arguing regarding claims 2 & 7 based on new limitations add, which has been address in the current Office Action using a new reference.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WARNER WONG whose telephone number is (571)272-8197. The examiner can normally be reached on 6:30AM - 3:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Warner Wong
Examiner
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/Kwang B. Yao/
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